CLAIMS

What is claimed is:

1. A method of programming a memory comprising:

sending a command to a memory device, said command requesting said memory device to enter a program mode;

sending a first address to said memory device;

sending a first packet of data to said memory device, said first packet of data to be programmed at said first address;

sending a first write signal to said memory device;

sending a second packet of data to said memory device; and

sending a second write signal to said memory device.

2. The method of claim 1 wherein said command is a fast program mode command.

3. The method of claim 1 further comprising sending a confirmation of said command.

4. The method of claim 1 wherein said first address is a starting address.

5. The method of claim 1 wherein said memory device is a flash memory.

6. The method of claim 1 further comprising sending a termination sequence to exit said program mode.

7. The method of claim 6 wherein said termination sequence comprises sending a data packet comprising all 1's to said memory device.

8. The method of claim 6 wherein said termination sequence comprises sending a second address to said memory device, wherein second address is different from said first

address.

9. The method of claim 6 wherein said termination sequence comprises sending a second address to said memory device, wherein said second address is the same as said first address.

10. The method of claim 1 wherein said first address is sent to said memory device as long as said memory device is in program mode.

11. The method of claim 1 further comprising polling a pin on said memory device to determine a status.

12. A method of writing data comprising:

receiving a command in a memory device, said command requesting said memory device to enter a program mode;

receiving a first address in said memory device;

receiving a first packet of data, said first packet of data to be programmed at said first address;

receiving a write signal;

programming said first packet of data to said first address;

incrementing said first address to a second address, said second address sequential to said first address;

receiving a second packet of data;

receiving a second write signal; and

programming said second packet of data at said second address.

13. The method of claim 12 wherein said command is a fast program mode command.

14. The method of claim 12 further comprising receiving a confirmation of said command.

15. The method of claim 12 wherein said first address is a starting address.

16. The method of claim 12 wherein said memory device is a flash memory.

17. The method of claim 12 further comprising receiving a termination sequence to exit said program mode.

18. The method of claim 17 wherein said termination sequence comprises receiving a data packet comprising all 1's.

19. The method of claim 17 wherein said termination sequence comprises receiving an new address in said memory device, wherein said new address is different from said first address.

20. The method of claim 12 wherein said command is received in control logic within said memory device.

21. The method of claim 20 wherein said control logic is a write state machine.

22. The method of claim 20 wherein said command causes said control logic to program data at sequential addresses in said memory device.

23. The method of claim 12 further comprising sending a status value from within said memory device to an output pin on said memory device.

24. An apparatus for programming a memory comprising:

a socket to receive a memory device, said memory device having a fast program mode; and

control logic coupled to said socket, said control logic to send code to said socket

to be programmed in said memory device coupled to said socket.

25. The apparatus of claim 24 wherein said memory device is a flash memory.

26. The apparatus of claim 24 wherein said fast program mode comprises receiving one address and a plurality of data packets.

27. The apparatus of claim 24 wherein said control logic polls a pin on said memory device for a status value.

28. The apparatus of claim 24 wherein said apparatus is a programmer.

29. A memory device comprising:

control logic to perform program operations in said memory device, said control logic having a fast program mode wherein said control logic receives one address value and a plurality of data packets;

a data bus coupled to said control logic;

an address bus coupled to said control logic;

a plurality of control signals coupled to said control logic; and

a memory array coupled to said control logic.

30. The memory device of claim 29 wherein said memory device is a flash memory.

31. The memory device of claim 29 further comprising a pin coupled to said control logic, said control logic sending a status value to said pin.

32. A machine readable medium having embodied thereon a computer program, the computer program being executable by a machine to perform a method comprising:

sending a command to a memory device, said command requesting said memory device to enter a program mode;

sending a first address to said memory device;

sending a first packet of data to said memory device, said first packet of data to be programmed at said first address;

sending a first write signal to said memory device;

sending a second packet of data to said memory device; and

sending a second write signal to said memory device.

33. The machine readable medium of claim 32 further comprising sending a confirmation of said command.

34. The machine readable medium of claim 32 further comprising sending a termination sequence to exit said program mode.

35. A computer system comprising:

a processor;

a bus coupled to said processor;

a user interface coupled to said bus; and

a socket coupled to said bus, said socket to receive a memory device having a fast program mode.

36. The computer system of claim 35 wherein said processor sends code to said memory device to be programmed.

37. The computer system of claim 35 wherein said memory device is a flash memory.